MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2015/2016

ECE2046 – COMPUTER ORGANIZATION AND ARCHITECTURE

(TE/EE/CE/ME/OPE/NANO)

4 MARCH 2016
9:00 a.m – 11:00 a.m.
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 7 pages including cover page with 5 Questions only.
2. Attempt **ALL** Questions. The distribution of the marks for each question is given.
3. Please print all your answers in the Answer Booklet provided.

Question 1

(a) The progress in IC technology development is reflected in Moore's law.

(i) State Moore's law.

[2 marks]

(ii) State **three** consequences of Moore's law.

[3 marks]

(b) Computers can be classified according to either their architecture or organization.

(i) Explain the meaning of computer architecture and computer organization.

[4 marks]

(ii) Draw a suitable diagram to represent the structure of a computer.

[2 marks]

(c) State and briefly explain three principal techniques for I/O operation.

[6 marks]

(d) Given that there are 32 words in the main memory where each word is 1 byte long. Also, given that there are a total of 16 lines in the cache where each line has 4 bytes. A set associative mapping function is to be implemented.

(i) How many blocks are there in the main memory?

[2 marks]

(ii) Given that 1 bit is reserved for the Tag field. Calculate the number of sets that are in the cache. Also, how many bits are reserved for the Word field?

[4 marks]

(iii) Subsequently, calculate how many lines are there in a set.

[2 marks]

Continued...

Question 2

(a) One of the functions of an operating system is to serve as a mediator, which provides programmers access to several services. List and describes three of such services.

[6 marks]

(b) Describe the operating approach employed in time-sharing systems.

[2 marks]

(c) Siti is assigned to design a virtual memory system that has a page size of 512 bytes, five virtual pages, and four physical page frames. The system should be able to map the following virtual address to their corresponding physical address.

Virtual Addresses	Physical Addresses
0	1024
2010	986
2049	1537
1026	Page Fault
707	195

(i) Can you explain to Siti the mapping concept between the virtual addresses generated by the CPU and the physical main memory addresses?

[4 marks]

(ii) Can you help Siti to create the page table for the system?

[5 marks]

Continued...

Question 3

(a) What is the benefit of using biased representation for the exponent portion of a floating-point number?

[2 marks]

(b) When does the arithmetic underflow problem in floating-point representation occur? Is the problem less serious than the overflow problem, and why?

[3 marks]

(c) Compute the following arithmetic operations in binary arithmetic using 8-bit two's complement notation. Comment on the discrepancies of the result, if any.

(i) $127_{10} + 1_{10}$

[3 marks]

(ii) $-39_{10} + 92_{10}$

[3 marks]

(d) Calculate the following floating-point arithmetic in binary form and store in IEEE 32-bit floating-point format:

$$3.625_{10} \times 10^{1}{}_{10} + 6.875_{10} \times 10^{-1}{}_{10}$$

[6 marks]

Continued...

Question 4

(a) Draw a diagram to illustrate the use of stack to implement the nested subroutine shown in Figure Q4(a).

[10 marks]

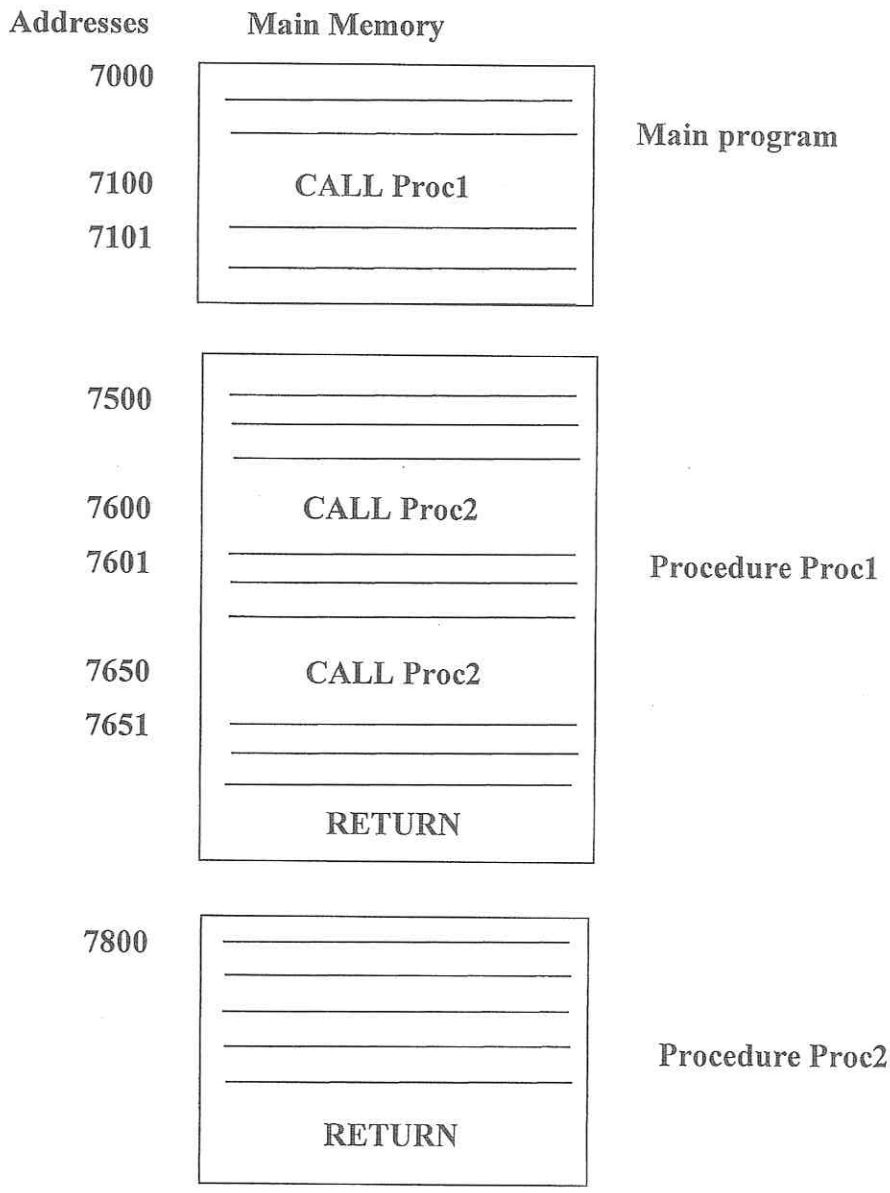

Figure Q4(a)

Continued...

(b) In a control unit, the instructions have to be broken down further into micro-operations.

(i) Describe the term micro-operations.

[3 marks]

(ii) Discuss the different usage of the four internal registers of a microprocessor: Memory Address Register (MAR), Memory Buffer Register (MBR), Program Counter (PC), and Instruction Register (IR).

[6 marks]

(iii) Write the possible sequence of micro-operations for the opcode ISZ X where ISZ stands for "increment and skip if zero".

[6 marks]

Continued...

Question 5

(a) Briefly explain the difference between pipelining and superpipelining architectures.

[1 mark]

(b) There are two superscalar architectures, namely, Complex Instruction Set Computer (CISC) and Reduced Instruction Set Computer (RISC). Which of the two is more complicated to implement? Justify your answer.

[4 marks]

(c) State 4 fundamental limitations to superscalar architecture.

[4 marks]

(d) Refer to the following assembly language program:

Instruction 1 : R3 = R1 + R2;
Instruction 2 : R4 = R3 + 1;
Instruction 3 : R3 = R5 + 1;

(i) Identify two instructions that have output dependency.

[2 marks]

(ii) Justify your answer in Q5(d)(i).

[2 marks]

(iii) State the name of the method that can be used to eliminate the dependency in Q5(d)(i) and explain how the method works.

[3 marks]

End of Paper